Link do produktu: https://www.gotronik.pl/emulator-mikrokontrolerow-avr-atmel-zgodny-z-jtagice-mk-ii-p-2857.html



Emulator mikrokontrolerów AVR Atmel zgodny z JTAGICE mk II

Cena brutto	999,00 zł
Cena netto	812,20 zł
Czas wysyłki	24 godziny
Numer katalogowy	JTAGICE-MKII

Opis produktu

Tis item is 100% compatible with Atmel's AT JTAGICE mkll, It supports AVR32 series of MCUs and can upgrade with avrstudio's upgrade tool.	
	Chip Didupping on all ASS, 8-NR. S-NR. SECC chromostrollers with THAS Interface or debugilIEE Interface, Clob have for a bit of supported devices.
ITAG The ITAG interface is a 4 wire Test Access Port (TAP) cor	trother that is complated with the IEEE 114-01 standard. The IEEE dandard was developed to enable a standard way to efficiently test cross board connectionly (Boundary Sans), Almed AVII devices have extended this functionality to include AUII Programming and Co-Chip Chipaging support.
The ITAGICE midII uses the standard ITAG interface to e	notion the user to do real time emoletion of the introsportinglier while it is nurring in the largest system.
The AVR On-Chip Debug (AVROCO) protocol gives the us	are compiled a colored of the sterned resources of the ARR intercontroller. Thus TIACICS relit gives accounts emulation at a fraction of the cost of traditional emulators.
SebugWIRE The debugWIRE interface adds a new way of doing On O	Dates. The delegiBBE Ch-chip delegi system uses a one-win, is directional interface to control the program flow, escale ANX instruction in the CNJ and to program the different non-visible memories.
When the debugWIRE Enable (DWEN) Fuse is programm	and and laid bits are un-programmed, the debugitTSE eyelem within the larged droce is activated. The RESET part pin is configured as a wire-AND (open-drant) is directional (I/O pin with pull-up enabled and becomes the communication palency between berget and enulator.
lote that debug/MSRC is a debugging interface only and	not a programming interface.
ISP the ITAGICE micil also supports full programming through	to the ISP interface. All TMS and debugliOSE garts are supported. See Programming with TMXISE mild for more information.
t works on either USB port or RS232 seriel port. ITAGICE mkII features	
	A OT Studies Commandation (AND Decision & 220 or Inter) A Special and A OT Decision and disciplings Studies A special and A OT Decision and disciplings Studies A special and A OT Decision and disciplings Studies A special and A OT Decision and disciplings Studies A special and A OT Decision and disciplings A Special And A Special
S-bit AVR: The JTACICE mkII also support devices with debugWIR The AVR Studio online-help contains the most current is	E historium, dubglittill evaluation on-thip debug of AVE representation in small pin count packages, using only a angle wine for the debug plantaux. **Termination and a committed limit of seconded delivers.**
Read more about AVR 8-bit RISC microcontrollers. 32-bit AVR32: The ITMGICE micil is supported by the AVR32 Studio. Read more about AVR32 32-bit NCU/DSP.	
AVR XMEGA Read AVR XMEGA from Atmel	
fore information, you can visit this urf from atmet's JTAGICE mid	
its://www.abmel.com/dyn/products/loois_card.aep?temily_id=60 Support Device:	Tillandy, person-VATE-M-473,2000-1822-4 date; g-2222
IVR 8-BIT MCU	
ATG: maps Selen: ATteguri ATmegal 2 ATmegal 2 ATmegal 4 ATmegal 18 A XTmegal 4 ATmegal 18 ATmegal 2 ATmegal 4 ATmegal 18 A XTmegal 28A1 ATmegal 4	Tempital Atmosfiliti Atmosfili
NebugWRE: maga Sariat: ATmaga SARIATANA ATMAGA ATM	Attraspatible Attraspatible Attraspation At
NVR 32-BIT MCU	
NATIG: AT32AP7000 AT32AP7001 AT32AP7002 AT32UC3A6128 AT3	ВЫСМИЗИ КТЕЙСЬКИЙ ИТЕЙСЬКИЙ ИТЕЙСЬКИЙ ИТЕЙСЕЙИЙ ИТЕЙСЕЙИЙ ИТЕЙСЕЙИЙ ИТЕЙСЕЙИЙ ИТЕЙСЕЙИЙ ИТЕЙСЕЙИЙ ИТЕЙСЕЙИЙ
Support "L" or "V" Serins Device, For example: ATmega*SL:: ATr Support Target Board VDD 2.1-6.5V The orbicard firmware is upgradeable via AVRStudio IDE to sup	regardEV got the edge Statistical disease.

